PATENT ABSTRACTS OF JAPAN

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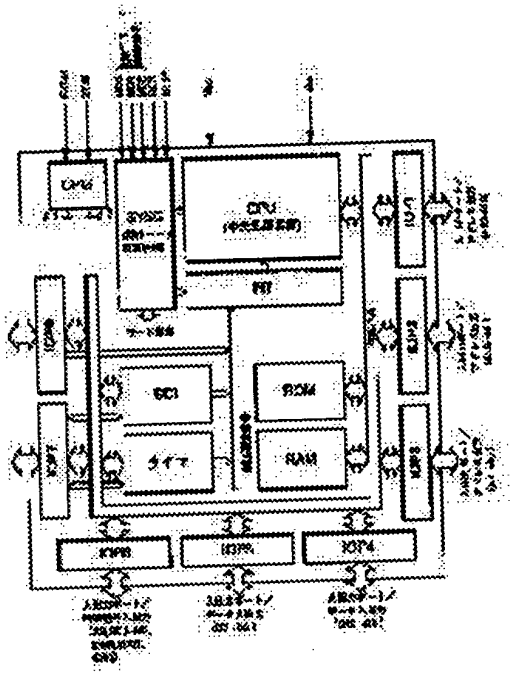
(54) DATA PROCESSOR

(57)Abstract:
PURPOSE: To provide the data processor which has many operation modes while increasing mode terminals, eliminating a decrease in the number of effective terminals, omitting the setting of a register means, and preventing the register means from being rewritten by mistake.
CONSTITUTION: This is a single-chip microcomputer which is formed as a semiconductor integrated circuit on one semiconductor substrate and consists of function blocks of a central processor CPU, a system controller SYSC, an interruption controller INT, a read-only memory ROM, a random access memory RAM, a timer, a serial communication interface SCI, 1st-8th input/output ports IOP1-IOP8, and a clock oscillator CPG. In initializing operation by hardware after this microcomputer starts operating, an operation mode is automatically read in and automatically set in a register.



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